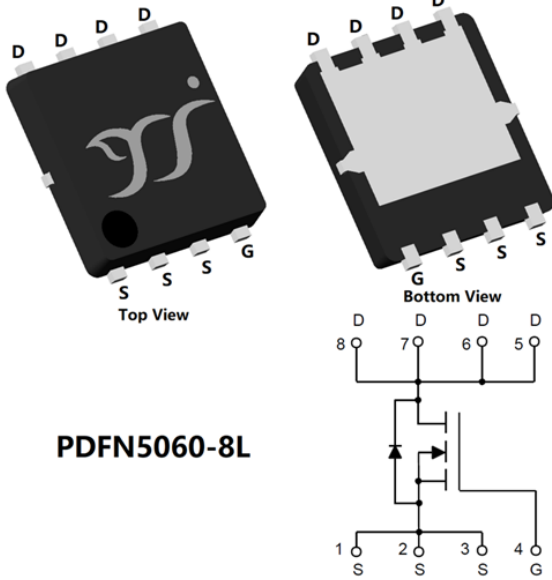


N-Channel Enhancement Mode Field Effect Transistor



PDFN5060-8L

Product Summary

- V_{DS} 40V
- I_D 300A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<0.9m\Omega$
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) $<1.4m\Omega$
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free
- Moisture Sensitivity Level 1
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V_{DS}	-	40	V
Gate-source Voltage			V_{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	$T_A=25^\circ C, V_{GS}=10V$	I_D	-	45	A
		$T_A=100^\circ C, V_{GS}=10V$		-	32	
Continuous Drain Current (Note 1,3)	Steady-State	$T_C=25^\circ C, V_{GS}=10V, \text{Chip limitation}$		-	300	
		$T_C=100^\circ C, V_{GS}=10V$		-	212	
Pulsed Drain Current	$T_C=25^\circ C, t_p \leq 10\mu s$		I_{DM}	-	1200	
Maximum Body-Diode Continuous Current	$T_C=25^\circ C$		I_S		135	
Avalanche energy (non-repetitive)	$T_J=25^\circ C, V_G=10V, R_G=25\Omega, L=4mH, I_{AS}=25A$		EAS	-	1250	mJ
Total Power Dissipation (Note 1,2)	Steady-State	$T_A=25^\circ C$	P_D	-	3	W
		$T_A=100^\circ C$		-	1.5	
Total Power Dissipation (Note 1,3)	Steady-State	$T_C=25^\circ C$		-	136	
		$T_C=100^\circ C$		-	68	
Junction and Storage Temperature Range			T_J, T_{STG}	-55	175	$^\circ C$

Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	50	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	1.1	

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG300G04ARQ	F1	G300G04AR	5000	10000	100000	13" reel



YJG300G04ARQ

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=1mA, T_j=25^{\circ}C$	40	-	-	V
		$V_{GS}=0V, I_D=10mA, T_j=25^{\circ}C$	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V, T_j=25^{\circ}C$	-	-	1	μA
		$V_{DS}=40V, V_{GS}=0V, T_j=100^{\circ}C$	-	-	100	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V, T_j=25^{\circ}C$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A, T_j=25^{\circ}C$	1	1.7	2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=50A, T_j=25^{\circ}C$	-	0.65	0.9	m Ω
		$V_{GS}=4.5V, I_D=20A, T_j=25^{\circ}C$	-	1	1.4	m Ω
Diode Forward Voltage	V_{SD}	$I_S=50A, V_{GS}=0V, T_j=25^{\circ}C$	-	0.78	1.2	V
Gate Resistance	R_G	$f=1MHz, T_j=25^{\circ}C$	-	2	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=20V, V_{GS}=0V, f=1MHz, T_j=25^{\circ}C$	-	6125	-	μF
Output Capacitance	C_{oss}		-	3250	-	
Reverse Transfer Capacitance	C_{riss}		-	150	-	
Switching Parameters						
Total Gate Charge	Q_g	$V_{GS}=10V, V_{DS}=20V, I_D=50A, T_j=25^{\circ}C$	-	101	-	nC
Gate-Source Charge	Q_{gs}		-	21	-	
Gate-Drain Charge	Q_{gd}		-	21	-	
Reverse Recovery Charge	Q_{rr}	$I_F=50A, di/dt=100A/\mu s, V_{GS}=0V, V_R=20V, T_j=25^{\circ}C$	-	94	-	nC
Reverse Recovery Time	t_{rr}		-	69	-	ns
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=10V, V_{DS}=20V, I_D=50A, R_{GEN}=3\Omega, T_j=25^{\circ}C$	-	16	-	ns
Turn-on Rise Time	t_r		-	44	-	
Turn-off Delay Time	$t_{D(off)}$		-	71	-	
Turn-off Fall Time	t_f		-	45	-	

Note:

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with $T_A=25^{\circ}C$. The maximum allowed junction temperature of $175^{\circ}C$. The value in any given application depends on the user's specific board design.
- Thermal resistance from junction to soldering point (on the exposed drain pad)



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Typical Electrical and Thermal Characteristics Diagrams

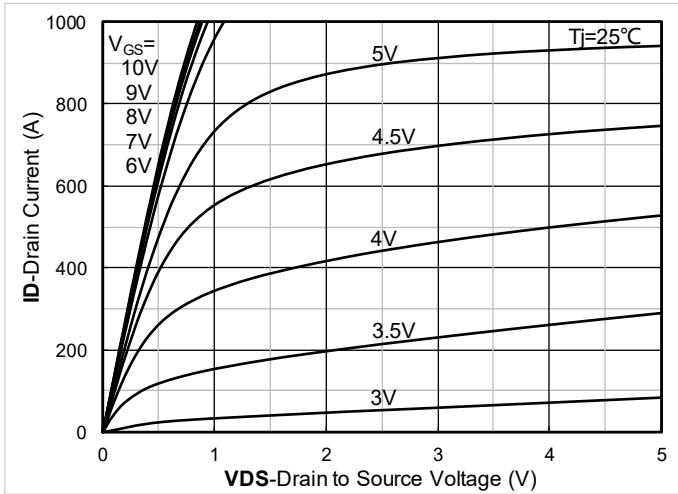


Figure 1. Output Characteristics

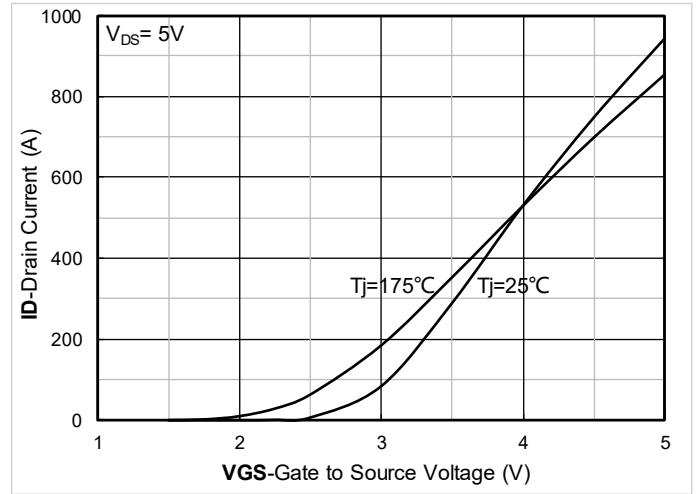


Figure 2. Transfer Characteristics

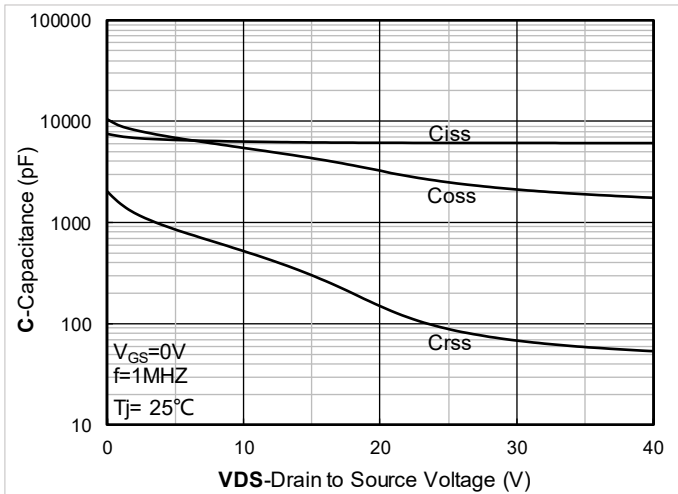


Figure 3. Capacitance Characteristics

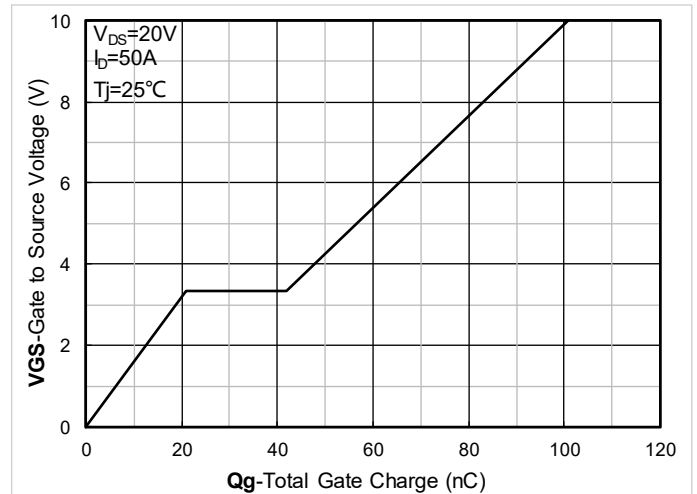


Figure 4. Gate Charge

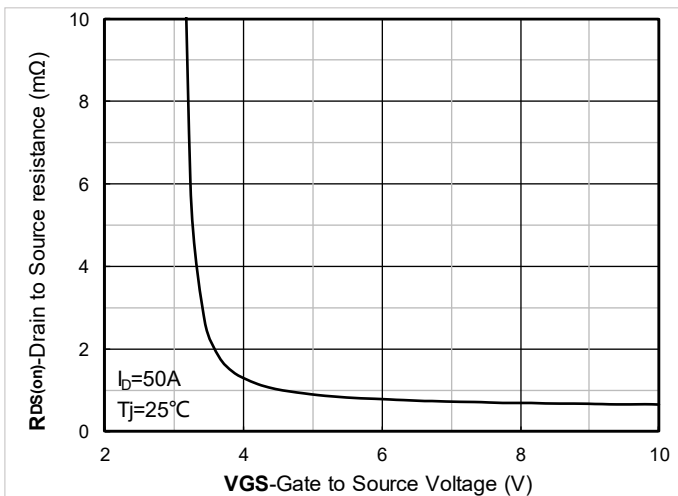


Figure 5. On-Resistance vs Gate to Source Voltage

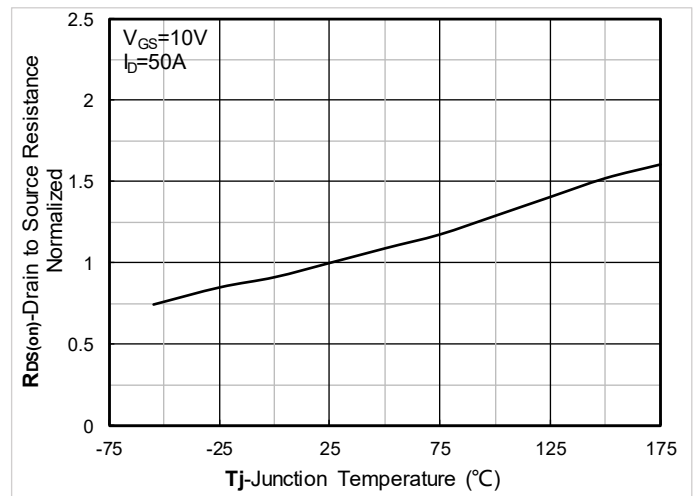


Figure 6. Normalized On-Resistance



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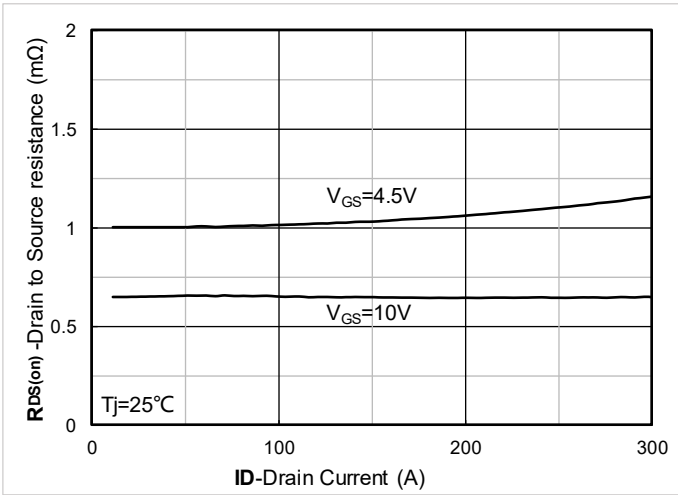


Figure 7. $R_{DS(on)}$ VS Drain Current

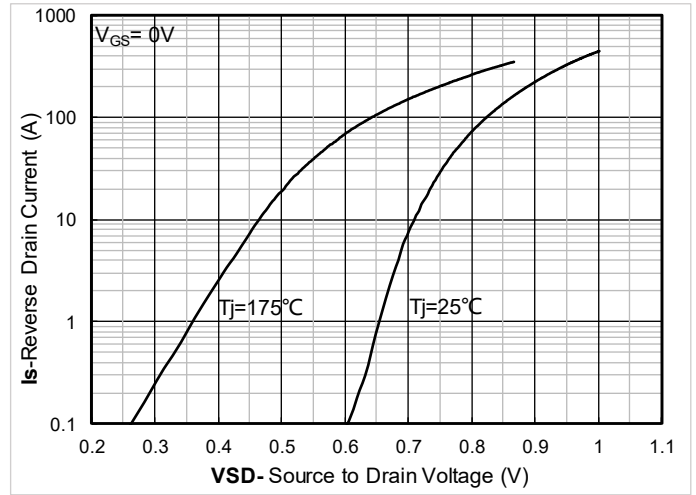


Figure 8. Forward characteristics of reverse diode

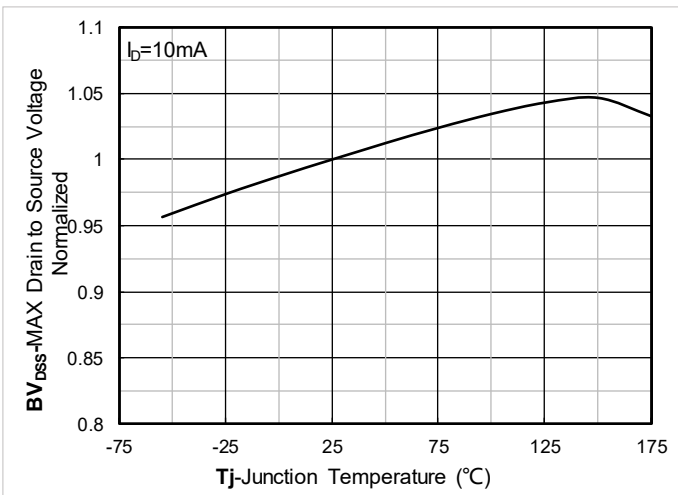


Figure 9. Normalized breakdown voltage

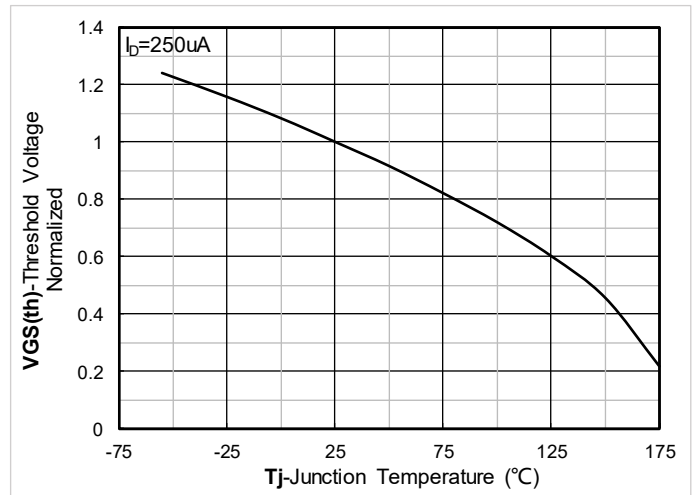


Figure 10. Normalized Threshold voltage

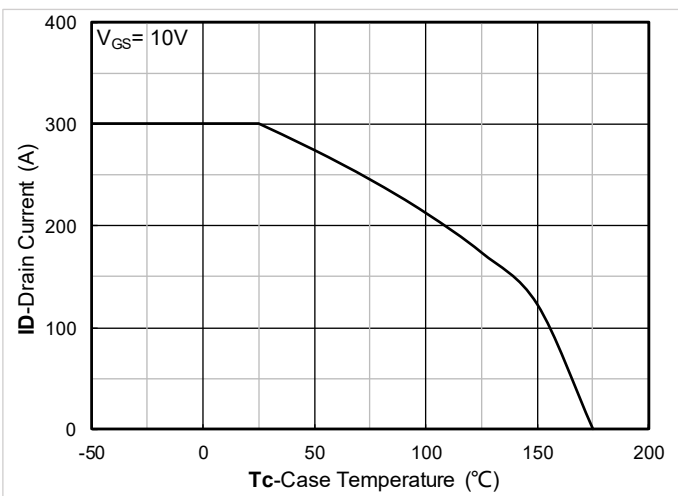


Figure 11. Current dissipation

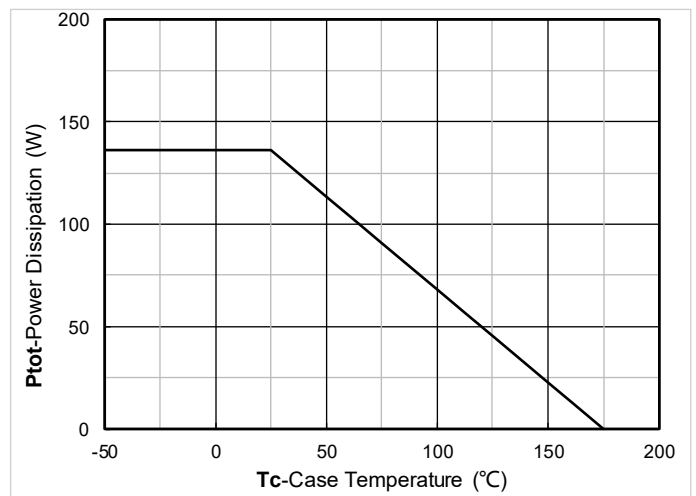


Figure 12. Power dissipation

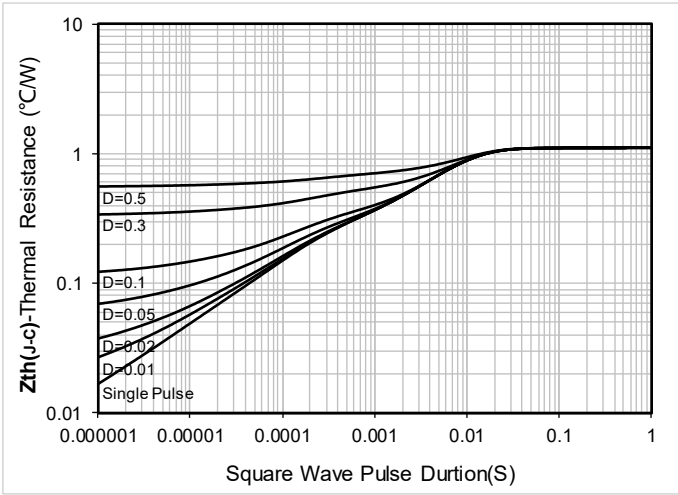


Figure 13. Maximum Transient Thermal Impedance

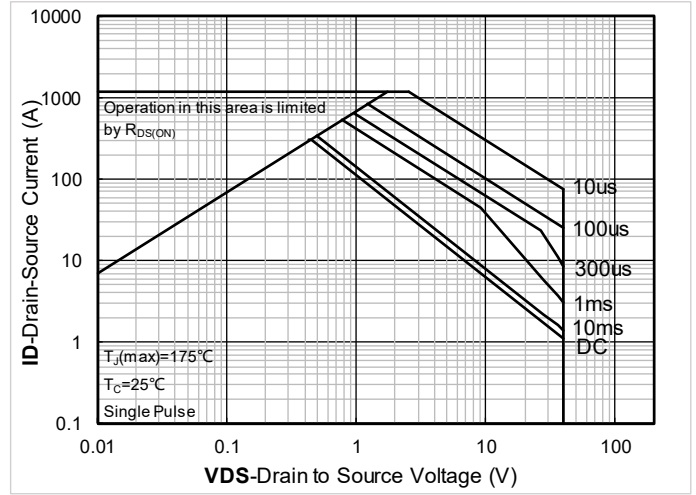


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

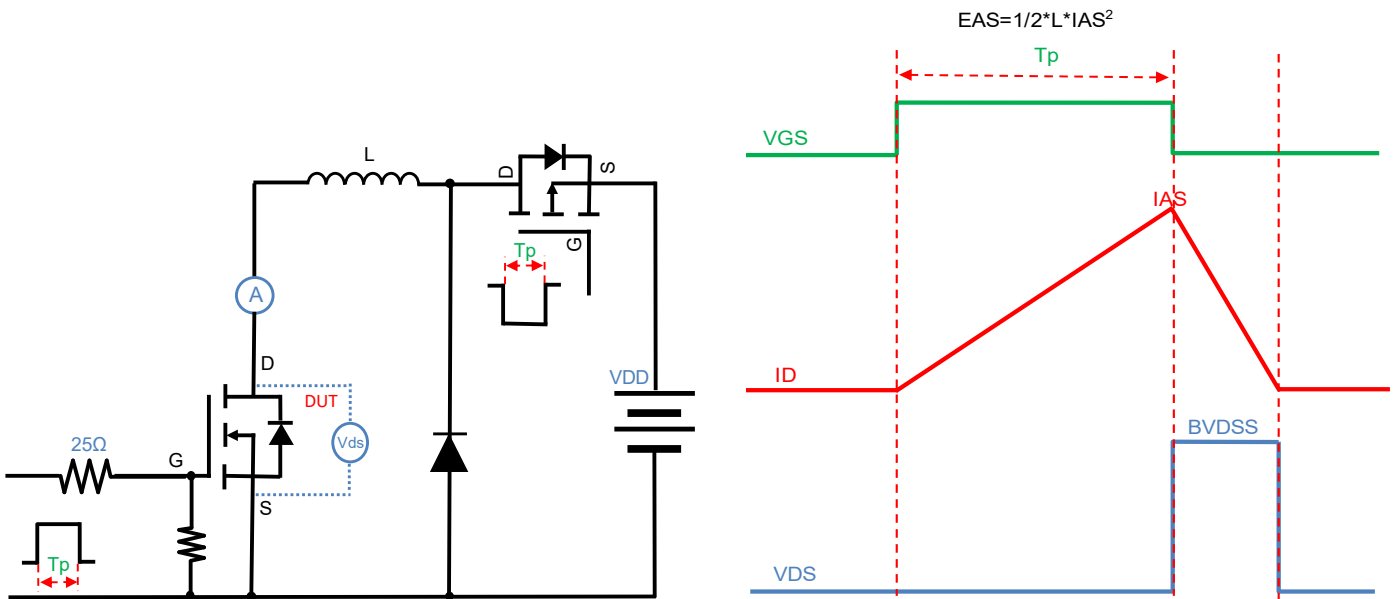


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

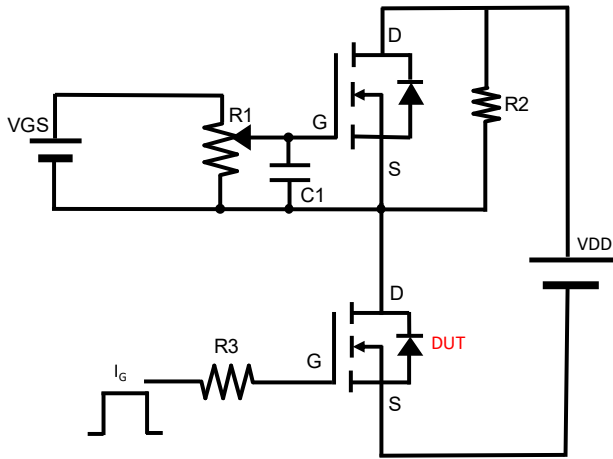


Figure B. Gate Charge Test Circuit & Waveform

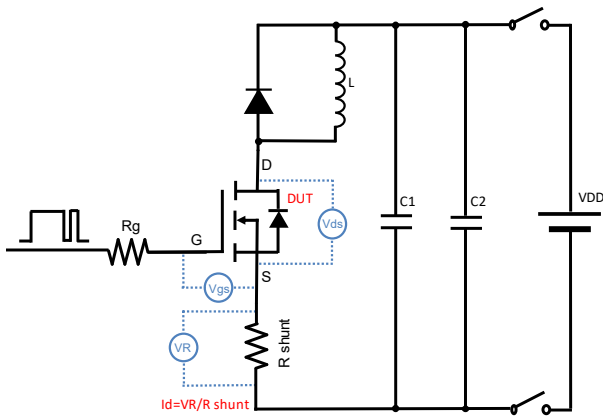


Figure C. Resistive Switching Test Circuit & Waveform

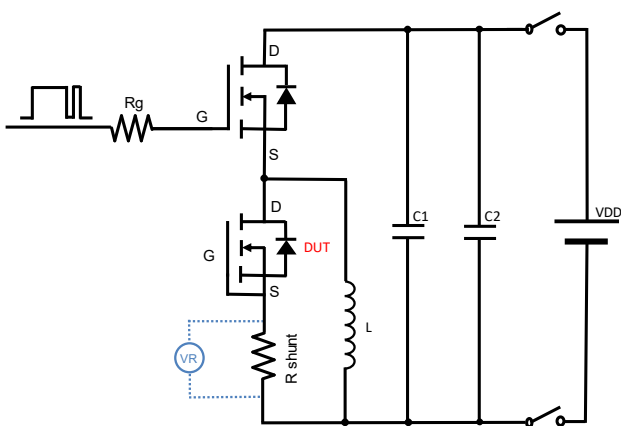
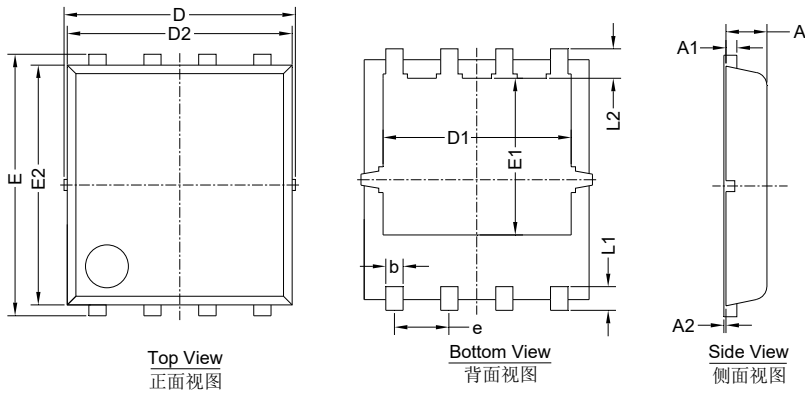


Figure D. Diode Recovery Test Circuit & Waveform

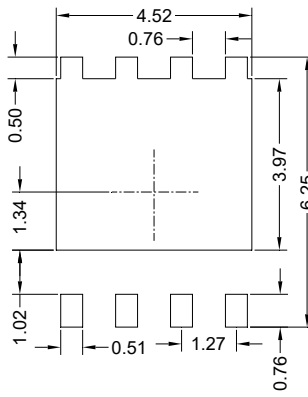


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■ PDFN5060-8L-D-0.95MM Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.05	6.15
A	0.85	0.95	1.00
A1	0.203 BSC		
A2			0.08
D1	4.25	4.35	4.45
E1	3.525	3.625	3.725
D2		5.20	
E2		5.55	
L1	0.45	0.55	0.65
L2	0.68 BSC		
b	0.3	0.4	0.5
e	1.27 BSC		



Note:
 1. Controlling dimension: in millimeters.
 2. General tolerance: ± 0.10 mm.
 3. The pad layout is for reference purposes only.



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